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CHRISTIE, PARKER & HALE, LLP
350 WEST COLORADO BOULEVARD
SUITE 500
PASADENA, CA 91105

EXAMINER	
LINNENKAMP, NICHOLAS L	

ART UNIT	PAPER NUMBER
2635	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/878,054	MCCORMACK ET AL.	
	Examiner	Art Unit	
	Nicholas L Linnenkamp	2635	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3,6,7*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 21, E2. Reference 21 is shown on Fig 2 but not described in the specification. Reference E2 is shown on Fig 5 but not described in the specification. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a) because they fail to show AL2-ALN, and PL2-PLN on Fig 5 and X1 and X2 on Fig 2 as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: The acronym PBRS is used on page 20 but not defined in the specification. It is unclear as to what PBRS represents in terms of relevant art.

Appropriate correction is required.

Claim Objections

The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claim 32 (second occurrence) through 43 has been renumbered 33 through 44. During the addition of new claims 23-43, two consecutive, different claims were given the number 32. The second claim 32 has been misnumbered and, as above, will be renumbered 33.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 32 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for having impedances at low frequencies according to the formula in the specification and claim and having impedance approximately unity at higher frequencies, does not reasonably provide enablement for having impedances approximately unity at all frequencies as specified by the claim. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

OK

The impedance corresponding to the first capacitance cannot be approximately unity and be approximately defined as according to the formula given in claim 32 at the same time unless resistances RS1 and RS2 are zero. It is understood that applicant most likely intended for the impedance of the precompensation filter to be equal to zero at "higher frequencies" but unless specified, such usage is not inherent in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4, 6, 13, 14,and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Dayton.

In reference to claim 1, Dayton teaches of a cross point switch unit (Fig 3) comprising a switch matrix module (Fig 2) with the switch matrix module comprising active elements (24, 28, 32, 34, 40a-d), transmission lines in one direction (20), and orthogonal transmission lines in a second direction (30). Dayton teaches of programmable registers (44) coupled to the active elements (40a-d), with the active elements coupled to one transmission line in one direction and on transmission line in the other direction. It is understood in the art that switch modules must have a programmable means to adjust the crosspoint connections through active elements.

In reference to claim 4, Dayton teaches that input lines (48) and output lines (50) are to be connected as signal lines (Col. 3, lines 35-36).

In reference to claim 6, Dayton teaches claim 4 as above. Dayton teaches of connecting a second switch matrix module (Fig 2) to the first matrix module with the output of the first matrix module connected to the input of the second matrix module (Fig 4).

In reference to claim 13, Dayton teaches claim 1 as above. Dayton teaches that a programming interface (70) can be connected to the switch core (78), and that output drive levels of the output of the switch matrix (40a-d) as commanded by the programming interface (70).

In reference to claim 14, Dayton teaches claim 1 as above. Dayton teaches that a programming interface (70) can be connected to the switch core (68) with output drive registers (44) coupled to the switch core, and that the switch core controls the output levels of the outputs (Fig 3).

In reference to claim 23, Dayton teaches of a crosspoint matrix with input lines (20) and output lines (30) coupled at certain points (40a-d) according to the shift register (78). It is understood that there is an insulating layer between input and output lines or the lines would come in contact with each other and incorrect operation of the crosspoint switch would result.

Thus Dayton teaches all the limitations of claims 1, 4, 6, 13, 14, and 23.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 2, 3, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dayton and prior art.

The examiner takes official notice that the method of making taps through photolithographic techniques falls within the scope of manufacture for integrated circuits. In addition, the connection of a generic substrate that has no defined purpose or attributes to the second element would fall within the scope of manufacture for integrated circuits. Constructing the tap using a different manufacturing process or connection of a substrate that does not provide any ascertainable difference as to the structure or functionality of the switch unit or switch matrix module does not constitute novelty.

In reference to claim 2, Dayton's teaches all the limitations of claim 1 as above in the 102(b) rejection. Dayton does not teach on the methods of connecting the cross point switch in terms of taps or via-holes. Dayton does teach that a monolithic IC switch can be constructed using photolithographic technology that is currently available (Col 3, lines 60-64). Photolithographic construction of taps and via-hole taps are available manufacturing processes.

In reference to claim 3, Dayton does not teach of generation of substrates during the manufacturing process of creating the switch. Coupling of a generic substrate to the orthogonal transmission lines would have been within the scope of typical manufacturing processes.

It would have been obvious to one skilled in the art at the time of invention to implement the teachings of Dayton with available technology because Dayton suggest such implementation (Col 3, lines 50-64), and the created switch is valid regardless of the manufacturing process used for the tap or the connection of generic substrates.

In reference to claim 15, Dayton does not teach the use of a secondary access port. It is well known in the art to include primary and secondary access ports. Such primary and secondary access mechanisms are known to include a console port, auxiliary port, and possibly a virtual terminal port through a telnet session.

An artisan skilled in the art at the time of invention would have included in the manufacture of the switch primary and secondary access systems as described above. It would have been obvious to one skilled in the art at the time of invention to include in the device of Dayton a primary and secondary access mechanism for controlling the crosspoint switch because a secondary access method would provide for greater flexibility in control such as having the ability to have two users programming the interface, or ability to remotely control the programming interface such as through telnet.

Thus Dayton and what is known in the art suggests all the limitations of claims 2, 3 and 15.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dayton in view of Heo et al (heretofore Heo). Dayton teaches claim 4 as above in the 102(b) rejection. Dayton teaches the connection of the switch modules to the substrate (102) but remains silent about the connection mechanism. Dayton does not teach of the inputs our outputs connected to the pads of a printed circuit board via a ball grid array (BGA). Heo suggest the use of a semiconductor package and assembly method. Prior art figure Fig 1B shows the connection of an IC to a substrate that connects through a BGA.

It would have been obvious to one skilled in the art at the time of invention to use the switch modules of Dayton (90, 92, 94, 96) in the prior art construction of Heo (Fig 1B) because Heo suggests that fabricating a semiconductor package in such a manner provides IC's that are light, thin, simple, and have a compact structure thereby providing an improvement in the integration degree and performance of the IC package (Col 1, lines 10-22).

Thus Dayton and Heo teach all the limitations of claim 5.

Claims 7-12, 24-28, 34-36, 38, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dayton in view of Morgan et al (heretofore Morgan).

In reference to claim 7, Dayton does not teach the use of a passive network coupled to the transmission lines. Morgan suggests the use of a low voltage amplification circuit that includes a passive network (16) connected to input lines (18, 21).

It would have been obvious to one skilled in the art at the time of invention to combine the teachings of Dayton with the suggestions of Morgan because Dayton teaches of a crosspoint switch for high-speed switching of data and Morgan teaches of an amplification circuit for use with high-speed data. In addition, Morgan suggests that such amplification circuits have such use in high-speed data transmission receivers (Col 3, lines 9-12).

In reference to claim 8, claim 7 is taught as above. Morgan suggests that the passive network (16) include capacitors (36, 43) and resistors (33, 41) tuned to

condition the signal for the respective voltages of a low voltage differential signal applied to the terminals (Col 3, lines 56-59).

In reference to claim 9, claim 7 is taught as above. Dayton teaches that input and output lines are coupled with a register (44). Moran suggests that the passive network includes a resistor (33 or 41) and capacitor (36 or 43) in parallel (Fig 1, 23) on each of the lines of a differential signal.

In reference to claims 10 and 11, claim 7 is taught as above. Placement of the Morgan's passive compensation network (16) on or off the die of the integrated circuit would have been within the scope of Morgan's invention because he describes the entire amplification circuit being implemented in an IC (Col 3, lines 7-9) and also provides that connection of any element, such as the passive compensation network (16), with other elements through direct connection on the same IC (Col 9, lines 37-41).

In reference to claim 12, claim 7 is taught as above. Morgan suggests that input circuit (16) is for conditioning high-speed data signals (Col 3, lines 9-12) and as such would inherently provide decreased signal attenuation at higher frequencies.

In reference to claim 24, claim 7 is taught as above. Morgan suggests the use of a differential signal path as shown by the differential signal applied to the terminals (Col 3, lines 58-59).

In reference to claim 25, claim 24 is taught at above. Morgan shows that the differential signal path includes a first (18) and second (21) transmission line with the passive network (23) comprising a resistance and a capacitance with a shunt resistor connecting first and second transmission lines. Morgan does not suggest the use of

multiple resistors or capacitors in series. It would have been obvious to one skilled in the art at the time of invention to place as many resistors or capacitors in series as would be necessary to achieve the desired resistance or capacitance of the compensation filter because choice of capacitance and resistance is a design choice.

In reference to claim 26, Dayton teaches of crosspoint switch unit with a first set of transmission lines (20) and a second set of transmission lines (30). Dayton does not teach of an amplifier chain coupled to the first set of transmission lines or a passive network coupled to the amplifier chain. Morgan teaches of an amplification circuit that includes an amplifier chain (12, 14, 17) with a passive network (16) coupled to the amplifier chain.

In reference to claim 27, Dayton and Morgan teach claim 26 as above. Dayton teaches that switching circuit may be implemented in a single monolithic integrated circuit (Col 3, lines 51-53).

In reference to claim 28, Dayton and Morgan teach claim 26 as above. Morgan teaches that passive network and amplifier chain may be implemented in an integrated circuit (Col 3, lines 7-9).

In reference to claim 34, Dayton teaches of a switch module. (Figs 2 and 3) Morgan teaches of a passive network having a predefined precompensation frequency response (23).

In reference to claim 35, claim 34 taught as above. Dayton teaches that switching circuit may be implemented in a single monolithic integrated circuit (Col 3,

lines 51-53). Morgan teaches that passive network and amplifier chain may be implemented in an integrated circuit (Col 3, lines 7-9).

In reference to claim 36, claim 34 taught as above. Morgan teaches that precompensation filter (23) is part of an amplifier section (12, 14, 17) that has a predefined amplifier frequency response. The passive precompensation filter (23) provides a predefined precompensation frequency response (Col 3, lines 51-59). It is understood that Morgan would have chosen a value for the capacitor such that Inter-symbol interference would be reduced so that faster switching could be supported of which the amplifier frequency response would have come into consideration, as a matter of common knowledge.

In reference to claim 38, claim 34 is taught as above. Morgan teaches that precompensation filter can be attached to input lines of a low voltage differential signal path for high-speed data switching, as taught above. It would have been obvious to one skilled in the art at the time of invention to place the precompensation filter on some or all inputs that would gain the benefit of lower inter-symbol interference.

In reference to claim 39, claim 38 is taught as above. The examiner takes official notice that Low Voltage Differential Signal (LVDS) lines are industry standards under ANSI/TIA/EIA –644 and IEEE 1596.3 SCI-LVDS.

Thus, Dayton and Morgan teach all the limitations of claims 7-12, 24-28, 34-36, 38, and 39.

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dayton in view of Shankar et al. (heretofore Shankar).

In reference to claim 16, Dayton does not teach of user registers coupled to the switch matrix module (Fig 2) for storing programming data provided by the programming interface (70). It is known in the art that all switches usually have some type of permanent storage to store programming in order to operate such as ROM, EPROM, EEPROM, or NVRAM. Shankar suggests the use of a programmable IC switch in which user registers (250) are provided for storing programming data provided by micro-controller (220). Such programming data is used for mapping information for setting the interconnections of inputs and outputs of the switch (120).

In reference to claim 17, Dayton does not teach of staging registers connected to switch matrix module (Fig 2), and for using programming interface to store programming data previously stored in the staging registers and providing it at a later time. Shankar suggests programming switch (120) through the micro-controller (220). It is well known that micro-controllers have output registers. Shankar suggests using output registers for programming switch and for storing data in user registers (250) for recalling later (Col 4, lines 54-57).

It would have been obvious to one skilled in the art at the time of invention to combine the teachings of Dayton with the suggestions of Shankar because Dayton teaches of a switch core and Shankar teaches of how to control a switch, and Shankar suggest that his programmable IC for manipulating a switch provides a simple and versatile programming process (Col 1, lines 45-54).

Thus, Dayton and Shankar teach all the limitations of claim 16 and 17.

Claims 18, 19, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dayton in view of Murata et al. (heretofore Murata).

In reference to claim 18, Dayton does not teach that the programming interface is configured to provide programming data that associates consecutive outputs to inputs as specified by the programming interface. Murata teaches of a programming interface (4) that provides programming data (S2) to a switch configuration management unit (5) that logically associates consecutive outputs to inputs as specified by programming interface (4).

In reference to claim 19, Dayton does not teach that programming interface is configured to group inputs and outputs of the switch matrix module. Murata teaches that programming interface provides programming data to management unit that logically groups inputs and outputs.

In reference to claim 21 and 22, claims 18 and 19 taught as above. Murata teaches that inputs and outputs can be logically associated in any manner desirable, logically or physically (Abstract).

It would have been obvious to one skilled in the art at the time of invention to combine the teachings of Dayton with the suggestions of Murata because Dayton remains silent about a programming interface, and Murata suggests a programming interface that uses a virtual control for associating input and output terminals. An artisan skilled in the art at the time of invention would have been motivated to combine

the teachings of Dayton with the suggestions of Murata because Murata's virtual control provides more efficient use of input and output ports (Col 1, lines 36-43). In addition, Murata discloses that prior art switchers input and output lines are arranged in the form of a matrix so that it is possible to switch the output destinations of the input signals or simultaneously distribute the input signals to a plurality of output lines in accordance with a user's instruction (Col 1, lines 16-21).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dayton and Shankar in view of Murata.

In reference to claim 20, Dayton and Shankar do not teach that programming interface can associate the groups of inputs to the groups of outputs. Murata teaches that groups of inputs can be logically associated with groups of outputs (Fig 10A, 10B).

It would have been obvious to one skilled in the art at the time of invention to combine the teachings of Dayton and Shankar with the suggestions of Murata because Dayton remains silent about a programming interface, Shankar provides the means for programming a switch such as the one disclosed by Dayton such as a micro-controller (220) and a PLD (250), and Murata suggests the use of a virtual control for associating input and output terminals. An artisan skilled in the art at the time of invention would have been motivated to combine the teachings of Dayton and Shankar with the suggestions of Murata because Murata's virtual control provides more efficient use of input and output ports (Col 1, lines 36-43). In addition, Murata discloses that prior art switchers input and output lines are arranged in the form of a matrix so that it is possible

to switch the output destinations of the input signals or simultaneously distribute the input signals to a plurality of output lines in accordance with a user's instruction (Col 1, lines 16-21).

Thus Dayton, Shankar, and Murata teach all the limitations of claim 20.

Claims 29-31, 37, and 40-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dayton in view of Morgan further in view of Huq et al. (heretofore Huq).

In reference to claim 29, Dayton and Morgan teach claim 26 as above. Morgan suggests that amplifier chain comprises a differential signal path (Col 3, lines 58-59) having a first (A) and second (B) signal path and the passive network comprises a first capacitance (36), a second capacitance (43), a first resistance (33), a second resistance (41) wherein the first resistance is coupled to the first capacitance in a first series path and the second resistance is coupled to the second capacitance in a second series path with the first series path coupled to the first signal path and the second series path coupled to the second signal path (Fig 1, 23). Morgan does not teach of a shunt resistance shunting the first series path to the second series path. Huq suggests that shunt resistors use is required in low voltage differential signal architectures to generate the differential output voltage (Page 2, LVDS Termination).

It would have been obvious to one skilled in the art at the time of invention to combine the teachings of Dayton with the suggestions of Morgan and Huq because LVDS termination is required in order to provide differential output voltage and Morgan

suggests a termination method (26). In addition, Huq suggests that simplicity and avoiding reflection problems are the main reasons to use single resistor termination (Page 2, LVDS Termination).

In reference to claim 30, claim 29 is taught as above. Dayton, Morgan, and Huq remain silent about impedance matching for first and shunt resistors with capacitors. Morgan suggests using any capacitance necessary to achieve proper signal conditioning (Col 3, lines 50-56). Given the resistance of Morgan, shunt resistance of Huq, and any capacitance value, a corner frequency could be found that would equalize the impedances, thus Dayton, Morgan, and Huq would exhibit the properties of claim 30.

In reference to claim 31, claim 30 is taught as above. Dayton, Morgan, and Huq remain silent as to having an impedance corresponding to the first capacitance being greater than the impedance corresponding to the first resistance at low frequencies generally less than the first corner frequency and the impedance corresponding to the first capacitance is greater than the impedance corresponding to the shunt resistance at high frequencies generally greater than the second corner frequency. Given the choice of any capacitance as described in claim 30 along with the desire to reduce inter-symbol interference, the system of Dayton, Morgan, and Huq would have exhibited the properties of claim 31.

In reference to claim 32, claim 30 is taught as above. Dayton, Morgan, and Huq remain silent as to the formulaic values of the impedance at low frequencies. As taught above in claim 31, given the choice of any capacitance along with the need to reduce

inter-symbol interference the system of Dayton, Morgan, and Huq would have compensated for its own internal resistors and thus exhibited the properties of claim 32. It is generally understood that applicant intended that the impedance corresponding to the first capacitance at "higher frequencies" approximately unity although applicant did not specify higher frequencies. The system of Dayton, Morgan, and Huq would have had an impedance of approximately unity at high frequencies.

In reference to claim 44, claim 30 is taught as above. Dayton, Morgan, and Huq remain silent as to having a capacitor frequency response approximately the inverse of the frequency response of the amplifier chain. Given the choice of any capacitance as described in claim 30, the system of Dayton, Morgan, and Huq would have exhibited the properties of claim 44. It would have been obvious to one skilled in the art at the time of invention to select a capacitance for a precompensation filter that would have reduced the Inter-symbol interface (ISI) including compensating for the distortion of the amplifying filters since Morgan suggests using a capacitance value to condition the incoming signal (Col 3, lines 50-56) and it is well known in the art that a reduction in ISI means that faster switching can be achieved.

In reference to claim 37, claim 34 is taught as above. Claim 37 is taught in a similar manner to claim 29.

In reference to claim 40, claim 34 is taught as above. Claim 40 is taught in a similar manner to claim 29. Morgan can be seen choosing similar resistances for resistors 33 and 41 and similar capacitances for capacitors 36 and 43.

In reference to claim 41, claim 40 is taught as above. Claim 41 is taught in a similar manner to claim 30.

In reference to claim 42, claim 40 is taught as above. Claim 42 is taught in a similar manner to claim 31.

In reference to claim 43, claim 40 is taught as above. Claim 43 is taught in a similar manner to claim 33.

It would have been obvious to one skilled in the art at the time of invention to select passive components in the precompensation portion of the amplifier chain described in Morgan so that the compensation circuit would have reduced inter-symbol interface as the object of the precompensation circuit is to emphasize high frequency components of the differential signal.

Thus Dayton, Morgan, and Huq teach all the limitations of claims 29-31, 37, and 40-44.

Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dayton, Morgan, and Huq further in view of Hilgenberg et al (Heretofore Hilgenberg). Claim 29 is taught as above. Dayton teaches that switching circuit may be implemented in a single monolithic integrated circuit (Col 3, lines 51-53). Dayton, Morgan, and Huq do not teach of using segmented, programmable resistors and capacitors. Hilgenberg suggests the use of fuse programmable electronic circuit for providing the desired resistance between two terminals. It would have been obvious to one skilled in the art at the time of invention to replace as necessary the resistors of Dayton, Morgan, and

Huq with the segmented programmable resistors of Hilgenberg because Hilgenberg suggests that programmable resistors are useful in applications where determination of a definite resistance value is only possible after final assembly of the completed circuit (Col 1, lines 12-19).

Thus Dayton, Morgan, Hug, and Hilgenberg teach all the limitations of claim 33.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nicholas L Linnenkamp whose telephone number is (703) 305-8701. The examiner can normally be reached on 8:00-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Horabik can be reached on (703) 305-4704. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4750.

Nicholas L Linnenkamp
Examiner
Art Unit 2635

NLL

MICHAEL HORABIK
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600